ABSTRACT OF THE DISCLOSURE

A data processing apparatus for executing multiple instruction sets. The apparatus includes a memory for storing a plurality of instruction words of the instruction sets, a processor core, for executing a primary instruction word of the instruction words, a program counter register (PC), for addressing a next instruction word stored in the memory, a plurality of data registers, for storing data of the instruction words, a processor status register, for storing the status of the processor core, wherein the processor status register contains an instruction set selector (ISS) for indicating a current instruction set of the instruction sets, a predecoder, for translating at least one of the instruction sets to the primary instruction word and outputting therewith, an Icache, for storing the primary instruction word, a decoder, for decoding the primary instruction word, wherein the processor core is used for executing the primary instruction word decoded by the decoder, a program counter control, responsive to the instruction set selector to modify the value of the program counter to fit the length of the instruction word different from the primary instruction word; and a bus interface, being an interface between the predecoder and the memory.